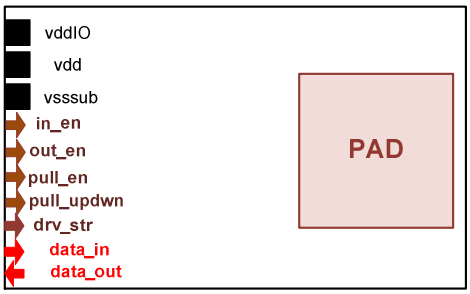
GPIO, LVDS and Analog Pad Library

Global Foundries 65nm LPe

CERTUS semiconductor
Custom IO and ESD Solutions

A 2.5V/1V Digital GPIO Library, that includes an LVDS PHY, and Analog/RF pads in Global Foundries 65nm LPe process.



FEATURES

VDDIO = 2.5V, VDD = 1.2V
Dual-row, staggered pitch of 45 um
Cell height 200 um, width 45 um
Outer bond pad opening: 60 um x 80 um y
Inner bond pad opening: 60 um x 60 um y
HBM 2000V
CDM 500V
MM 200V
Junction temp range: -40C to 125C

LVDS TX and LVDS RX Features

1.5Gb Data rates
Self-Biased, no reference blocks needed
Flexible Power/GND pads arrangements
allow for very dense LVDS IO placement
without Compromising Signal Integrity
Complies with ANSI/TIA/EIA-644-A
Also supports various non-standard LVDS electrical specs

Analog and low-Cap RF pass-through cells (ESD protected)

GPIO Standard Features

200MHz operation for 10pF Loads
150MHz operation for 15pF Loads
Standard Output and Input Enable
Selectable pull-up or down termination resistors
Dynamically Selectable drive strength: 12mA and 24mA
Complies with JEDEC JESD 8-5 LVCMOS Specs

SUMMARY

The GPIO pad set provides basic digital IO cells and the associated IO power, core digital power, and ground cells with built-in ESD circuits. This pad set also has macro blocks implementing LVDS TX and LVDS RX circuits. There is a stand-alone Analog/RF cell that passes-through an ESD protected analog/RF signal. Current footprints and formats comply with minimum dimensions for Global Foundries packaging requirements. The IO Libraries are exceptionally reliable from an ESD perspective, and are in fact capable of exceeding 4kV HBM and 800V CDM, however such levels of ESD qualification depend more on final padring construction, as opposed to achieving a standard 2kV HBM and 500V CDM qual.

MODELS and SUPPORT FILES

GDS Layouts
LEF Abstracts
CDL netlist for simulation and LVS
Liberty Timing files
Functional models in behavioral Verilog with timing arcs.

FRONT-END DEVICES

Uses 2.5V NMOS, PMOS, diodes for IO circuits, 1.2V NMOS, PMOS for core interface circuits. No ESD Implant layer is used, as well as no other special masks, only base mask set is required.
Back-end: M1, M2-M6 (1x metal), B1 (2x), EA (4x), LB (bond pad metal)

VARIANTS

A Metal Option 14 variant, which changes the back-end metal busing.

There is a 3.3V variant which uses 3.3V NMOS, PMOS, and diodes. The GPIO is designed to remain completely functional at 2.5V at spec performance of 150 MHz at 10 pF output load. Performance may be higher at 3.3V VDDIO. This variant integrates the Metal Option 14 backend.

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