Certus Semiconductor Process Experinence

Process Technology	Full Custom IO and Padlib Library IP	Customized IO Designs	Full ESD Library IP	Custom ESD Solutions	Consultation: IO and ESD Design	Consultation: ESD Debug Efforts
TSMC 12nm	1.8V, 3.3V and 5V IO Libs					
TSMC 16nm	1.8V, 3.3V and 5V IO Libs					
TSMC 22nm	1.8V, 3.3V and 5V IO Libs					
TSMC 28nm	1.8V, 3.3V and 5V IO Libs					
TSMC 40nm	1.8V, 3.3V, 5V and >20V IO Libs					
TSMC 65nm	1.8V, 3.3V, 5V and >20V IO Libs					
TSMC 90nm						
TSMC 130nm	1.8V, 3.3V, 5V and 6.5V IO Libs					
TSMC 180nm	1.8V, 3.3V, 5V and >20V IO Libs					
TSMC 250nm						
GF 22nm FD-SOI						
GF 45nm						
GF 65nm	1.8V, 3.3V and 5V IO Libs					
GF 180nm	1.8V, 3.3V and 5V IO Libs					
SMIC 40nm						
SMIC 65nm						
IBM SOI/RF 180nm						
Samsung 28nm FD-SOI	1.8V, 3.3V and 5V IO Libs					
IBM/Samsung 32nm						
IBM/Samsung 45nm						
UMC 55nm						
Peregrine/Silanna 250nm	1.8V, 3.3V and 5V IO Libs					
Peregrine/Silana 500nm	1.8V, 3.3V and 5V IO Libs					
Lfoundry 110nm	1.8V, 3.3V IO Libs					
Silterra 130nm						
TSI 250nm BCD						
Various JAZZ						
Various XFAB						
Various Vanguard						

Key

Yes:If IP related, publicly available		
Yes: If IP related, not publicly available. Contract Design		
No		