MULTI-VOLTAGE GPIO WITH HDMI, LVDS AND ANALOG PADS LIBRARY

TSMC 28NM HPM/HPC/HPC+

CERTUS semiconductor
CUSTOM IO AND ESD SOLUTIONS

A 1.8V to 3.3V/0.9V Digital GPIO Library, which includes an HDMI, LVDS, Analog/RF Low capacitance and 5V Open-drain and ESD pad set in TSMC N28 HPM/HPC processes.

FEATURES

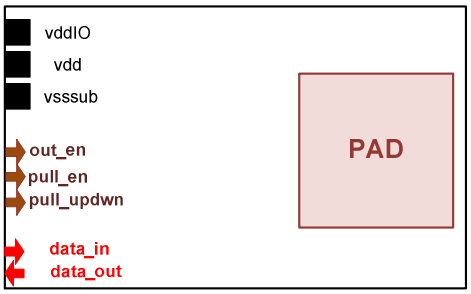
VDDIO = dynamically selectable 1.8V, 2.8V or 3.3V
VDD = 0.9V
Dual-row, staggered pitch of 25um
Cell height 130um, width 25um
Outer bond pad opening: 44um x 55um y
Inner bond pad opening: 44 um x 55um y
Shorted Output Protection
HBM 3000V
CDM 800V
MM 300V
IEC 2kV*
Junction temp range: -40C to 125C
Can integrate with TSMC standard IO

5V Open-Drain IO and ESD Protection

Open-Drain IO for I2C, CEC, DDC, VBUS and similar applications
1.8, 3.3 and 5V operational ranges supported
Fail-Safe IO
Low Leakage

HDMI and LVDS Pad Features

Are not PHYs, but are bondpads with ESD and Powers
Includes Power and GND pads
<250fF per IO including Bondpad
1.8V to 3.3V Power supply *(HDMI)*
1.8V Power Supply *(LVDS and analog)*
5V Tolerant *(HDMI only)*
Fail-Safe IO *(HDMI only)*
Pad Macros provide for ideal parasitic matching between differential signal pins.



GPIO Standard Features

***System** can dynamically change VDDIO from 1.8V to 2.8V to 3.3V during operation; IO will adjust and meet performance spec. Allows for a broader customer base with one IO and chip design.*
3 Classes of GPIO give designers options for optimizing performance, power and noise
150MHz operation for 10pF Loads
75 MHz operation for 10pF Loads
25 MHz operation for 10pF Loads
Full Speed Output-enable for open drain applications.
Selectable pull-up or down termination resistors
Complies with JEDEC JESD 8-5 LVCMOS Specs
2kV IEC robust
Shorted output protection

Analog and low-Cap RF pass-through cells (ESD protected)

Low capacitance options from <100fF to 500fF (includes Bondpad)
Full ESD Compliance

SUMMARY

The DGIO28HPM pad set has digital cells that can drive spec loads at 25 MHz, 75 MHz, and 150 MHz, allowing you to manage SSO currents and peak power. Digital pads can be configured as input, full output, open source, open drain, with or without an internal 50K ohm pullup or pulldown. Pad cells for IO Power, Ground, Core Power, with built-in ESD circuits are in the set. A key feature is that the VDDIO supplies can be selected and dynamically changed during operation in the system. All digital IO and power pads will detect voltage range and adjust accordingly to meet spec. This gives product designers greater flexibility when targeting customer systems. The IO are also robust to 2kV IEC 61000-4-2 system stresses, beyond the regular HBM, CDM and MM. The Analog subset includes a low-cap pass-through Macros LVDS signals, standard analog/RF pads, AVDD and AVSS cells with ESD protection,. Transition cells are included to integrate analog segments of the pad ring with the digital sections; this is necessary to complete the ESD protection architecture. There is an HDMI Macro block with very low capacitance signal pads with built-in ESD. The HDMI VDD and VSS pads are built-in within the macro and transition cells also integrate the macro with the rest of the pad ring. The HDMI pads are 3.3V compliant, Fail-Safe and 5V tolerant. The pad Library includes a large number of variant cells to allow for extremely flexible padring constructions, while maintaining rigorous ESD protection. The variants include feed-through and high current power supply pads. The Library is silicon proven and currently in production.

MODELS and SUPPORT FILES

GDS Layouts
LEF Abstracts
CDL netlist for simulation and LVS
Liberty Timing files
Functional models in behavioral Verilog with timing arcs.

FRONT-END DEVICES

1.8V Thick-oxide NMOS and PMOS; 0.9V thin oxide NMOS and PMOS and diodes. No ESD Implant layer or special masks required.
Back-end: Supports a variety of BEOL options, native design is for staggered wirebond, but also flip-chip compliant.

VARIANTS*

A non-IEC compliant pad set exist that is 110um tall, also has reduced shorted output protection.
Other variants include special macro cells that allow for alternate bonding package options where the customer can bondout either HDMI/LVDS signals, or GPIO's. Only sacrifices 60um cell height.
Can be modified for Flip-Chip applications. 2kV IEC compliance is also dependent on system design.

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