3D IC integration and ESD: "Not the ESD you grew up with!"

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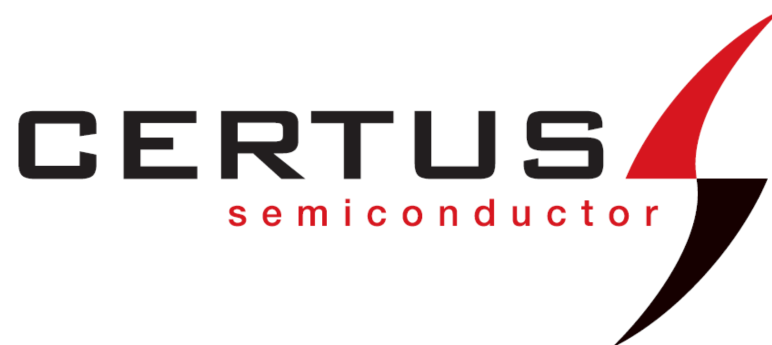

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Founder of SRF Technologies, a Certus Member, and custom IO and ESD Design Service. Has been designing custom IO libraries and ESD circuits, specializing in RF and specialty analog IO's both in IC's and Systems for over 15 years.

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The Big Question

- Does 3D IC integration make ESD a bigger problem?

This is what everyone wants to know.

(As is true in most things, its neither a yes nor no)

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3D IC Integration and ESD

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Partition the question:

Are there new ESD threats to the IC caused by 3D integration?

How are current ESD design practices impacted by 3D integration?

Are the current ESD models and test standards still applicable?

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3D IC Integration and ESD

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Are there *new* ESD threats to the IC caused by 3D integration?

There are two new obvious items:

- Backside wafer thinning to expose TSV's
- Additional ESD risk due to new Assembly steps such as Die-to-Die Bonding, Package-to-Package Stacking, etc.

These two processes are unique to 3D IC…to some degree.

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3D IC Integration and ESD: Backside Wafer Thinning

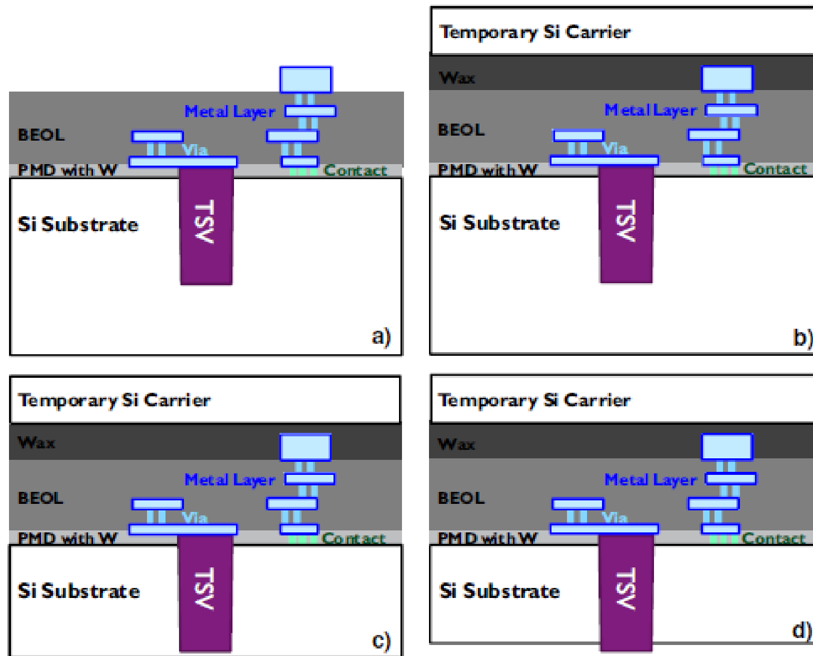

Figure 1: Processing steps in wafer thinning process module: (a) after the front-side manufacturing, (b) temporary Si carrier mounting, (c) wafer thinning by wet grinding or dry polishing, and (d) recess etching and TSV exposing for back-side connection.

1. Shih-Hung Chen; Thijs, S.; Linten, D.; Scholz, M.; Hellings, G.; Groeseneken, G., "ESD protection devices placed inside keep-out zone (KOZ) of through Silicon Via (TSV) in 3D stacked integrated circuits," *Electrical Overstress/Electrostatic Discharge Symposium (EOS/ESD), 2012 34th*, vol., no., pp.1,8, 9-14 Sept. 2012

- Process necessary to expose TSV's is a new step relative to standard 2D IC.
- Wet Grinding: Liquid can allow for less accumulation of ESD charge.
- Dry Polish: More susceptible to ESD charge accumulation.
- TSV connected circuits are susceptible to any plasma charging that can occur during recess etching.

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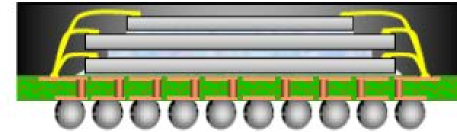
3D IC Integration and ESD: Assembly Risks

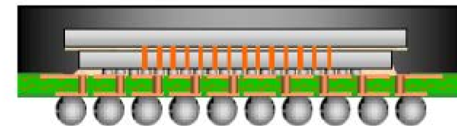
- Assembly risk vary by nature of the technology.

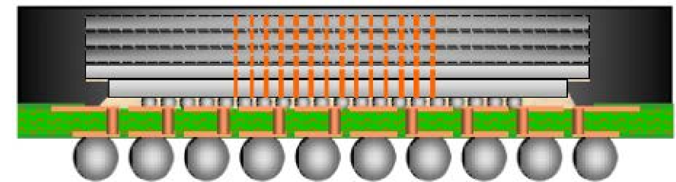
Stacked Wire-Bond (WB) IC's are not new or unfamiliar to us. Assembly risk are no different than current WB processes.

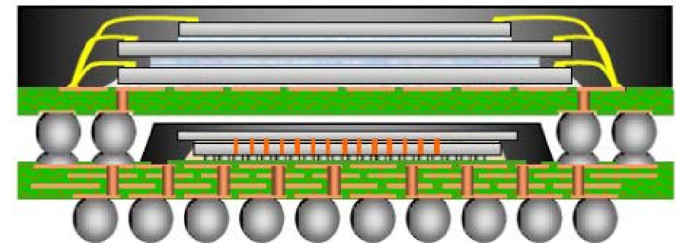
Stacked IC's utilizing TSV's are a newer approach and do have some risks in assembly that "maybe" new.

Multi-Chip module packages are definitely not new, but we are not taking advantage of the technology to minimize ESD impacts on design.









3D IC Integration and ESD: Assembly Risks

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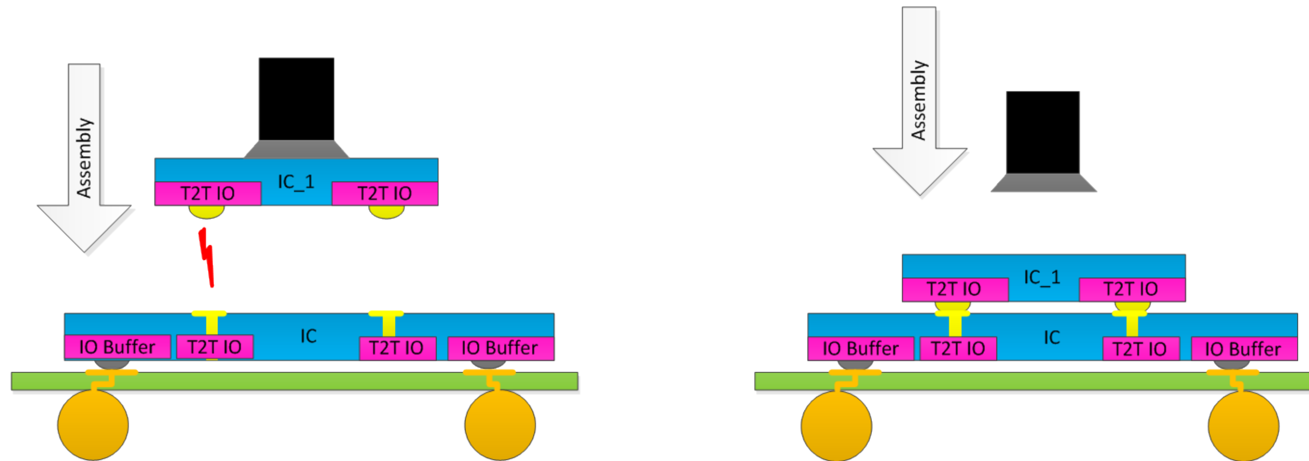

During the die stack, the very first TSV to come in contact will act as a discharge path to equalize currents between the two die to be encapsulated.

This is very representative of a CDM event but there are a few major differences.

1. Bare die have low charge
2. Unless the bottom die is hard grounded, CDM peak current will be minimal
3. Die stacking assembly will likely have better ESD controls than a typical PCB pick and place assembly station.

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3D IC Integration and ESD: Assembly Risks

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- Reality regarding 3D IC assembly ESD risks:

  The new assembly processes present no "*new*" ESD risks that are not already managed or experienced by current flip-chip or wire bond technologies.

  The particular type of risk due to assembly is a CDM (Charged Device Model) following ESDA/JEDEC standard.

  Generally, Peak Currents during assembly will be significantly lower than traditional PCB assembly.

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3D IC Integration and ESD: Assembly Risks

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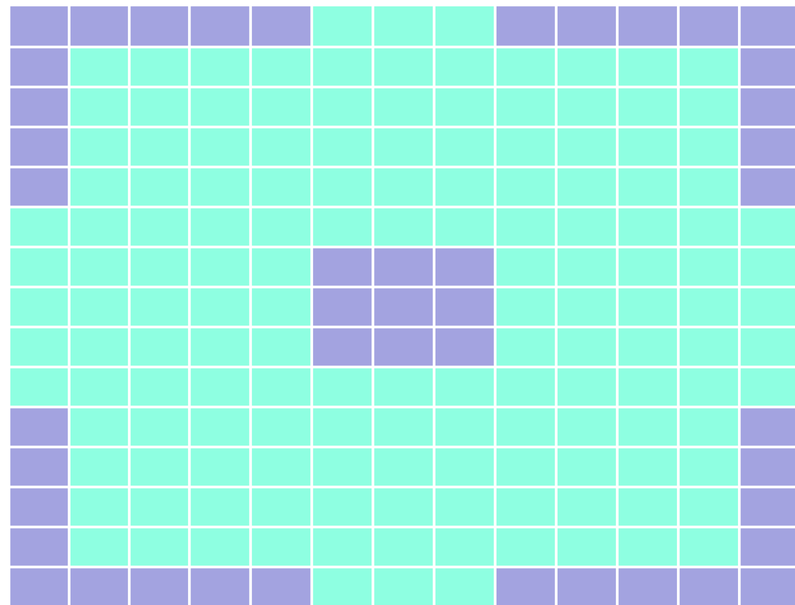
- Side Comment

It is possible to control CDM currents during by taking advantage of the statistical reality of “first TSV contact”

Only corner, edge and center balls will make first contact during assembly. (Private study)

Active T2T Buffer TSV’s

Grounded TSV's to ensure first contact for CDM discharge



The only problem with such an approach is it may requires extra TSV’s.

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3D IC Integration and ESD: ESD Design Practice

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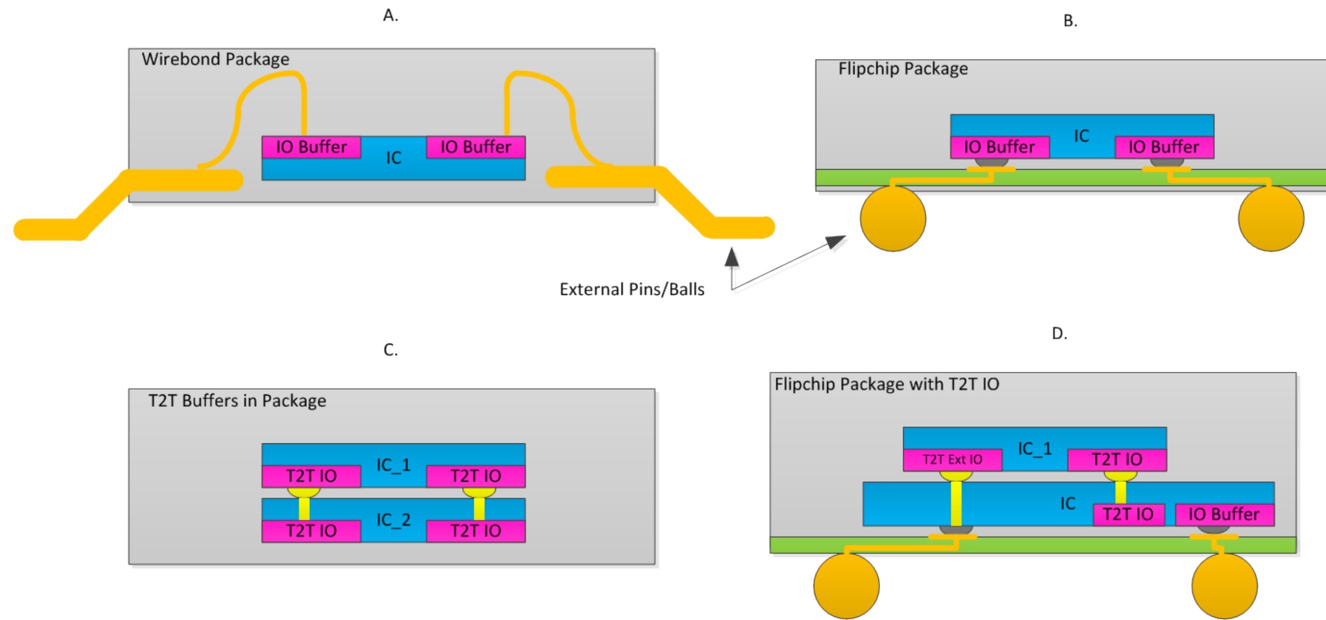
- ESD Design for 3D IC's creates a whole new realm of IO design considerations.



Not every Tier-to-Tier (T2T) buffer has an external package connection. Not every T2T buffer then may need full ESD design.

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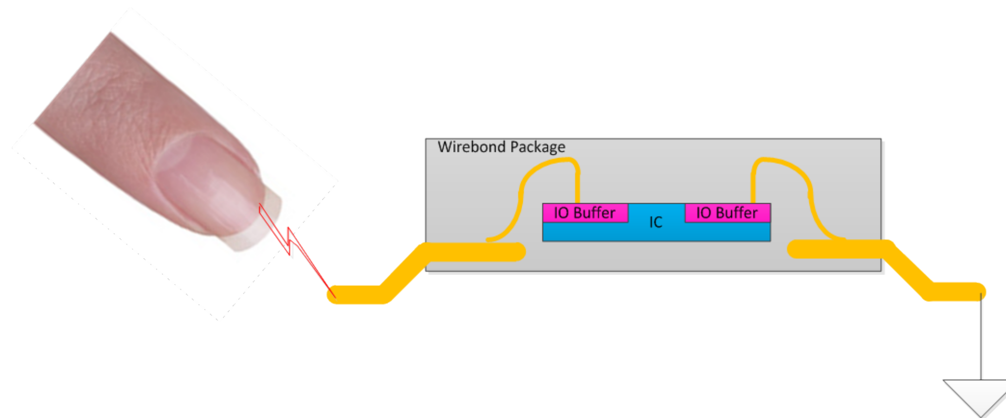
3D IC Integration and ESD: ESD Design Practice

- ESD Events for a packaged part only directly occur on external pins.



Simplistic HBM Concept

- Only those pins with external IO will experience or be tested directly for ESD events.

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- Key Realities about T2T/TSV Buffers

Once package, internal only T2T Buffers will likely not experience a full or direct ESD events

Internal T2T Buffers cannot be tested by Normal ESD Standards

-An exception being wafer level ESD testing or specialized packages for ESD testing.

-Currently the only Commercial ESD Test Lab capable of doing wafer level HBM/MM Testing is a new ESD Test Facility “Minotaur Labs”.

For those interested contact Adam Bergen: abergen@minotaurlabs.com

-There does not exist any current systems for wafer level CDM (and it doesn’t make sense either)

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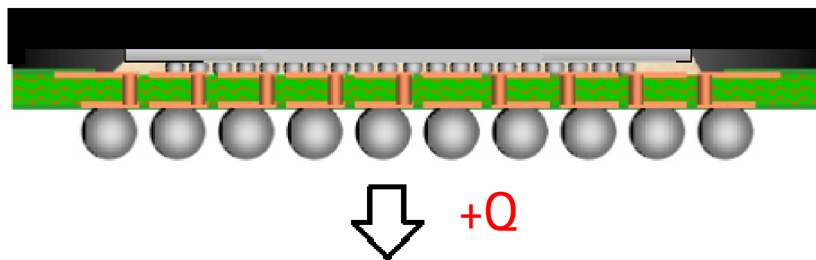
- CDM will worsen

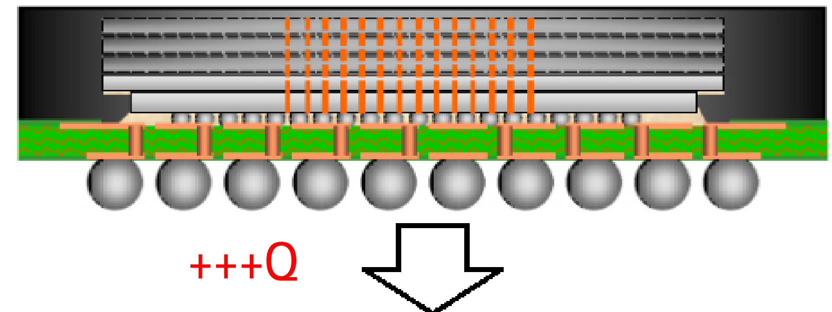
  CDM peak currents during assembly of the 3D IC to PCB's will likely increase due to additional Package size/circuits/interconnect.

  CDM currents will find a path between every IC in the stack and the external Pins.

  CDM design for 3D IC's must consider signal power domain crossings for internal T2T and TSV buffers between IC's just like is currently practiced with SoC designs.

  The Key to robust CDM design will lie in a correct ESD architecture for all power/ground domains of the 3D stack as a whole.





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❒ Design Impacts

- Not Every TSV Buffer will need a full ESD protection circuit.

  -Only those buffers with External Package Pins will.

  -Internal Buffers may be allowed a dramatically reduced ESD protection.

  -Current paths must still be architected through the entire 3D Package

- HBM/MM will only apply to external Pins.
- CDM Currents will worsen for external pins and the IC stack
- Internal T2T or TSV buffers may or may not experience a dangerous ESD threat during CDM. Depends on the coordinated ESD of all integrated IC's
- CDM robustness will require a 3D IC Package to have accounted for proper CDM current paths between all IC's and external pins.

-This can be mitigated largely by proper grounding between IC's

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New Concepts that have been played with in actual silicon:

Dramatically reduced ESD where appropriate for reduced TSV/T2T IO footprint.

Collective CDM current handling

-using multiple TSV/T2T buffers to “share” IC to IC CDM currents.

TSV power grids designed for both power delivery to the TSV Buffer array but also architected ESD current paths between IC’s in a 3D stack.

ESD dedicated TSV’s for mitigated CDM currents in 3D IC assembly as well as PCB system assembly.

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3D IC Integration and ESD: ESD Testing

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- ESD testing and models have been discussed indirectly so far.
- Key Items to note about HBM/MM* testing:
  - HBM/MM* testing can only occur on a packaged part, or wafer if using specialized equipment/Labs such as Minotaur Labs.
  - Bare die sold as is for assembly in a 3D IC may not have an HBM spec unless they are tested using the specialized equipment or an ESD only package.
  - Once Packaged internal TSV connections can not be directly tested for HBM/MM* compliance.
  - HBM/MM* events will only occur on external signals and possibly internal connections between die if the external Pin to external Pin path requires currents pass through internal TSV connections.
    - This will completely hamper the ability to find failing connections between die by curve trace unless full disassembly occurs of the 3D IC.
    - Debugging of HBM failures of the 3D IC could be as difficult as current CDM debug is.
    - Only ATE testing will truly help uncover internal failures.

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3D IC Integration and ESD: ESD Testing

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- Key Items to note about CDM testing:
  - CDM testing can only occur on a packaged part. Wafer level is impossible.
  - Bare die sold as is for assembly in a 3D IC may not have a CDM spec unless they are tested using an ESD/debug package.
    - The ESD package may or may not reflect the CDM performance of the die in the 3D IC.
    - CDM peak currents are dominated by package size, design, pin counts and #IC in the package.
  - Once Packaged internal TSV connections can not be directly tested for CDM compliance.
  - CDM events will only initiate on external signals but CDM currents will flow in every IC of the 3D stack.
  - CDM failures are system architecture dependent
    - CDM Failures can occur on a die in a 3D stack that were not present when tested individually.

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3D IC Integration and ESD: ESD Testing

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- **And you thought ESD debug in a normal package was tough…**
  - Try finding failure emissions in a 3D stack…
  - ESD Current paths must be architected and coordinated across all IC's in a 3D stack.
  - Which IC failed during CDM events?
    - Internal failures will not register with curve trace on external pins
    - Failures will require full ATE test flow and the ability to intelligently isolate failures.
  - It is hard enough to debug ESD when your entire product database is accessible by the product team.
    - Now try doing ESD debug when the silicon designs of each IC are independently owned by separate companies.
    - Just because a die passed individual testing doesn't mean it will pass in the 3D IC
    - Who is to blame? Who coordinates the final CDM/HBM current path designs?

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3D IC Integration and ESD: Conclusion

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- No new stresses are added to the system that we do not already understand/manage.
- ESD design now has more flexibility in that not every IO buffer needs full ESD protection, specifically if it is a T2T interface and does not connect to an external pin.
  - Intelligence and the 3D system understanding must be applied when deciding which buffers can utilize reduced ESD structures.
  - Brute force approach is to design every IC/Buffer with full ESD protection…but this will waste a LOT of area.
- HBM ESD Current paths are easier to architect
  - External pin to external pin.
- CDM ESD Current paths are harder to understand
  - Package dependent, so individually passing dies may fail in the 3D stack
    - 3D IC will have higher peak CDM currents that individual dies in testing.
  - Currents will flow between every IC and signal in the design
  - 3D IC architecture must account for CDM currents

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3D IC Integration and ESD: Conclusion

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- The biggest challenge for ESD and 3D IC's
- HINT: It isn't typical product level ESD design or the added risks from 3D assembly
- Its coordinated ESD design between product teams
  - Coordinated ESD Architecture of the individual IC's for the 3D IC
    - Never historically accomplished
    - The equivalent is trying to design system level ESD but for Charged Board Model (CBM) and not just CDM.
  - ESD Debug will be a nightmare
    - Failures will likely be a combination of architectural decisions that were made by independent companies/suppliers.
    - Coordinating the debug between multiple component suppliers will not be fun

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1. Shih-Hung Chen; Thijs, S.; Linten, D.; Scholz, M.; Hellings, G.; Groeseneken, G., "ESD protection devices placed inside keep-out zone (KOZ) of through Silicon Via (TSV) in 3D stacked integrated circuits," *Electrical Overstress/Electrostatic Discharge Symposium (EOS/ESD), 2012 34th* , vol., no., pp.1,8, 9-14 Sept. 2012

*: Machine Model (MM) testing though still common in the industry is not encouraged or recommended. It is an incorrect standard that causes false failures that are not likely to occur in the real world.

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