HDMI, LVDS, RF and Analog Pads Library

TSMC 45nm/40nm Process Families

CERTUS semiconductor
Custom IO and ESD Solutions

A 1.0V to 5V Analog IO Library that includes an HDMI, LVDS and Analog/RF Low capacitance pad set in TSMC 45nm/40nm HPM processes.

FEATURES

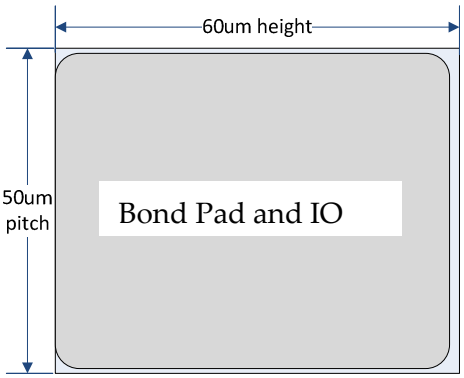
In-Line Low-Cap Analog: 50um pitch x 60um height
(HDMI, LVDS, RF, Analog and Low-Cap IO's)
Dual-row, staggered pitch of 25um x 150um height
(Analog, RF, LVDS and Low-Cap IO's)

AVDD = 1.0V to 3.3V nominal, 5V tolerant HDMI option
Capacitance 150fF to 250fF including Bondpads*
HBM >4000V*
CDM >800V*
MM >300V*
IEC >2kV option*
EOS protection
Junction temp range: -40C to 125C
Can integrate with TSMC standard IO

HDMI and LVDS Pad Features
Are not PHYs, but are bondpads with ESD and Powers
Includes Power and GND pads
<250fF per IO including Bondpad
1.8V to 3.3V Power supply *(HDMI)*
1.8V Power Supply *(LVDS and analog)*
5V Tolerant *(HDMI only)*
Fail-Safe IO *(HDMI only)*
Pad Macros provide for ideal parasitic matching between differential signal pins.

Analog and low-Cap RF pass-through cells (ESD protected)

WORLDS SMALLEST IN-LINE IO FOOTPRINT!!



The entire HDMI, RF and Analog In-Line cells are only 2.2um taller than the bond pads, completely CUP (Circuit Under Pad) and providing the industries smallest footprint for RF, Analog and HDMI Low-Cap ESD and Pad solutions.

SUMMARY

The DG40 Analog IO set is a collection of analog only IO and Power/Ground pads that include ESD. The target applications are high performance analog interfaces including HDMI, RF, LVDS, basic analog and other applications. The pads include a host of specialty features including fail-safe, low cap, high ESD protection and even IEC robustness. The IOs's are also deisgned to trigger and protect interfaces during EOS (Electrical Overstress events) during normal operation. A key feature of the library is the extremely small footprint of the inline IO set, only 2.2um bigger than the bond pad itself. Capacitance can range from <150fF to 250fF and is scalable based on the customers' needs between ESD robustness and capacitive loading.

MODELS and SUPPORT FILES

GDS Layouts
LEF Abstracts
CDL netlist for simulation and LVS
Functional models in behavioral Verilog with timing arcs.

FRONT-END DEVICES

2.5V overdriven 3.3V Thick-oxide NMOS and PMOS; No ESD Implant layer or special masks required.
Back-end: Metal1 to Metal8, AP bondpad layer for wirebond, using Circuit-Under-Pad construction.

***: Capacitance and ESD robustness is a sliding scale, customers opting for lower capacitance do so at a cost of ESD robustness, and vice-versa. Nominal ESD numbers listed are for 200-250fF Capacitive IO structures.**

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