1.8V/3.3V SWITCHABLE GPIO WITH 5V I2C OPEN DRAIN & ANALG IN TSMC 16FF/12FFC TECHNOLOGY

CERTUS semiconductor
CUSTOM IO AND ESD SOLUTIONS

TSMC 16nm & 12nm Flip-Chip IO library with dynamically switchable 1.8V/3.3V GPIO, 5V I2C / SMBUS open-drain cell, 5V OTP cell, 1.8V & 3.3V analog cells, and associated ESD.

SUMMARY

A key attribute of this library is its ability to detect and dynamically adjust to a VDDIO supply of 1.8V or 3.3V during system operation. The GPIO cell can be configured as input, output, open-source, or open-drain with an optional internal 50K ohm pull-up or pull-down resistor. Four selectable drive strengths are offered (25-235MHz @1.8V, 10pF) to optimize across SSO currents & power. The output driver exhibits 50Ω (±20%) termination across PVT to reduce reflections at higher operating frequencies. Supply cells for VDDIO, VREF, and core VDD include necessary built-in ESD circuitry. A 5V I2C / SMBUS open-drain (fail-safe) cell, 5V OTP programming gate cell and 1.8V & 3.3V analog cells with ESD protection are included. The library features protection break cells to allow for separate grounds while maintaining ESD robustness. ESD design targets are 2KV HBM, & 500V CDM, yet this library has consistently demonstrated 4KV HBM. This library can also support 2KV IEC 61000-4-2 system ESD with appropriate integration.

OPERATING CONDITIONS

Parameter	*Value*
VDDIO	1.8 / 3.3V selectable
VREF	1.8V
Core VDD	0.8V
Tj	-40°C to 125°C
Max_Load	50pF (10pF at speed)

CELL SIZE & METAL STACK

Cell size	*Metal Stack*	*Package Type*
30x50um	1P8M 1P10M	Flip-Chip

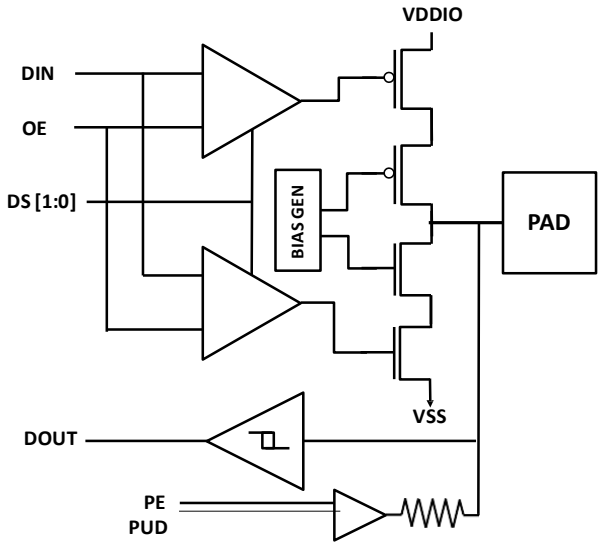
LIBRARY CELL SUMMARY

Cell Type	*Feature*
Supply / ESD	1.8/3.3V; 1.8V; 0.8V; GND
GPIO[1]	25-235MHz, selectable
I2C Open-drain[2]	5V, fail-safe
Analog	1.8V & 3.3V
OTP	5V programming gate cell
Break cells	VDDIO, VDD, VSS

DRIVE STRENGTH PERFORMANCE @10pF

DS [1:0]	*1.8V*	*3.3V*
00	25 MHz	15 MHz
01	140 MHz	75 MHz
10	200 MHz	150 MHz
11	235 MHz	175 MHz

GPIO BLOCK DIAGRAM



GPIO FEATURES

- Multi-voltage 1.8V / 3.3V switchable operation
- 4 selectable drive strengths (25-235MHz @1.8V, 10pF)
- Full-speed output enable
- Independent power sequencing
- 50Ω (±20%) source termination across PVT
- Schmitt trigger receiver
- 50KΩ selectable pull-up or pull-down resistor
- ESD: 2KV HBM, 500V CDM[3], 2KV IEC 61000-4-2[4]
- Silicon proven

Certus also supports IO libraries in the following TSMC nodes: 180nm, 130nm, 110nm, 65nm, 55nm, 45/40nm, 28nm, and 22nm. Additional Certus libraries are available across technologies supported by Global Foundries & Samsung. Certus is particularly suited at providing custom variants in a cost-efficient framework. Feel free to inquire for supplementary physical or electrical features to suit your needs.

1. GPIO speeds are load dependent (faster for lighter loads, slower for heavier). Speeds shown are at 10pF. Up to 400MHz (1.8V), & 250MHz (3.3V) at 5pF.
2. Open drain cell is I2C, SMBUS, DDC, CEC, & HPD compliant.
3. CDM rating is a function of package size. Rating shown is for nominal packages.
4. Please contact a Certus representative for IEC 62100-4-2 protection levels achievable with your design.

