1.2 – 1.8V GPIO WITH ULTRA-LOW LEAKAGE, LOW-CAP, 1.8V/5V & 20V – 36V HV ANALOG IN TSMC 180nm TECHNOLOGY

CERTUS semiconductor
CUSTOM IO AND ESD SOLUTIONS

A TSMC 180nm Flip-Chip IO library with 1.2-1.8V GPIO, 1.8V & 5V RF analog, OTP program cell, 20-36V ultra-low leakage low-cap HV analog & associated ESD

SUMMARY

This library is particularly tailored to address gaps in the native foundry IO offerings for this node. It features a 1.2-1.8V GPIO with selectable dual drive strengths and optional internal 105KΩ pull-up or pull-down resistor. Supply cells for IO and core power include necessary built-in ESD circuitry. The analog suite includes 1.8V & 5V low-cap RF analog cells & ESD with optional substrate isolation, an OTP-program cell tolerant up to 7.5V, and an ultra-low leakage, low capacitance 20-36V HV analog cell. The library is enriched with filler, corner, domain break, and secondary CDM cells to allow for flexible segment construction. This library is silicon- proven and robust to 2KV HBM & 500V CDM.

OPERATING CONDITIONS

Parameter	*Value*
VDDIO	1.2-1.8V (1.8V nom)
Core VDD	1.2-1.8V (1.2V nom)
Tj	-40˚C to 125˚C
Max_Load	15pF | 30pF (DS=0|1)

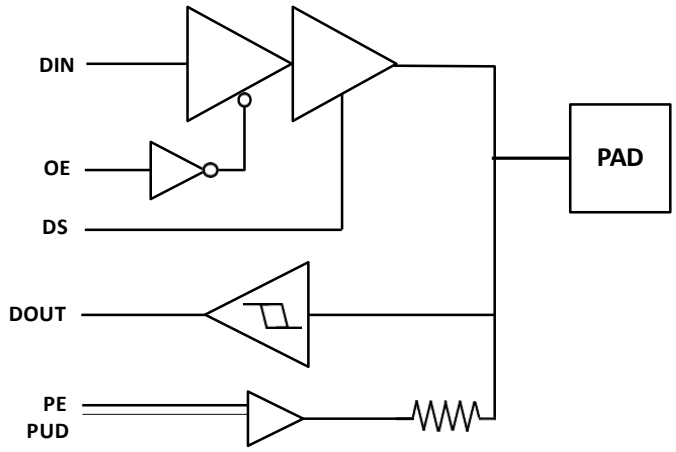
CELL SIZE & METAL STACK OPTIONS

Cell size	*Metal Stack*	*Package*
60x80um	6M_1MN_RDL	Flip-chip

LIBRARY CELL SUMMARY

Cell Type	*Feature*
Supply / ESD	1.8V IO, 1.2V core [nom]; GND
GPIO[1]	50MHz (dual load select)
1.8V Analog	Substrate isolation option
5V RF Analog	Substrate isolation option
20-36V HV	Ultra-low leakage, low-cap[2]
Break cells	VDDIO, VDD, VSS
Filler cells	1um, 5um digital & analog
Corner	Digital & analog
CDM protect	Internal & secondary

GPIO BLOCK DIAGRAM



GPIO FEATURES

- 1.2V-1.8V operation (IO & core)
- Selectable 15pF | 30pF load support options at 50MHz
- Schmitt trigger receiver
- 105KΩ selectable pull-up or pull-down resistor
- ESD: 2KV HBM, 500V CDM[3]
- Silicon-proven

Certus also supports IO libraries in the following TSMC nodes: 130nm, 110nm, 65nm, 55nm, 45/40nm, 28nm, 22nm, and 16/12nm. Additional Certus libraries are available across technologies supported by Global Foundries & Samsung. Certus is particularly suited at providing custom variants in a cost-efficient framework. Feel free to inquire for supplementary physical or electrical features to suit your needs.

1. GPIO can sustain 50MHz at 15pF loads when DS=0, and 30pF when DS=1
2. Leakage target <1nA, capacitance <350fF
3. CDM rating is a function of package size. Rating shown is for nominal packages. Certus IOs typically handle 10-20A Peak CDM currents, depending on IO type.

