1.8V/3.3V SWITCHABLE GPIO WITH I2C, HDMI & LVDS ESD & ANALG IN TSMC 28nm HPM/HPC/HPC+

CERTUS semiconductor
CUSTOM IO AND ESD SOLUTIONS

A TSMC 28nm HPM/HPC+ Wirebond IO library with dynamically switchable 1.8V/ 3.3V GPIO, 5V I2C open-drain, 1.8V& 3.3V analog cells, OTP cell, HDMI & LVDS protection macros & associated ESD - featured across a variety of metal stack and pad configuration options.

SUMMARY

A key attribute of this library is its ability to detect and dynamically adjust to a VDDIO supply of 1.8V or 3.3V during system operation. The GPIO cell set can be configured as input, output, open-source, or open-drain with an optional internal 60K ohm pull-up or pull-down resistor. Digital cells for 25MHz, 75MHz, and 150MHz allow optimization across SSO currents & power. Cells for I/O & core power & ground with built-in ESD circuitry are included. The library also features 5V I2C open-drain (fail-safe), 5V OTP programming cell, and 1.8V & 3.3V analog cells with ESD protection. 1.8V LVDS and 3.3V, 5V tolerant fail-safe HDMI protection blocks with low-cap signal pads are also available. The library is enriched with feed-through, filler, transition and domain-break cells to allow for flexible pad ring construction. This library is silicon-proven and robust to 2KV HBM / 500V CDM and is 2KV IEC 61000-4-2 system level capable.

OPERATING CONDITIONS

Parameter	*Value*
VDDIO	1.8 / 3.3V selectable
VREF	1.8V
Core VDD	0.9V
Tj	-40°C to 125°C
Max_Load[1]	50pF (10pF at speed)

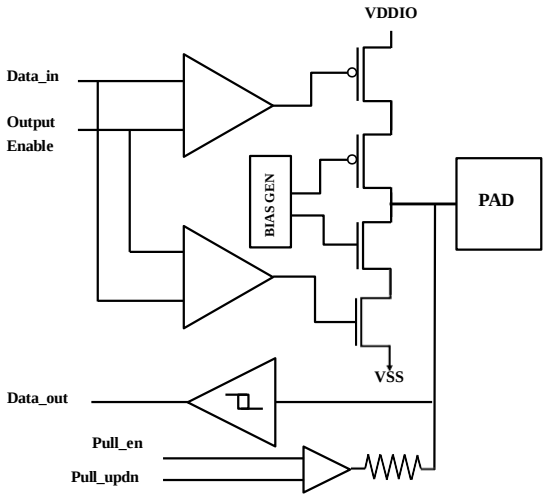
CELL SIZE & METAL STACK OPTIONS

Cell size	*Metal Stack*	*Wirebond Pitch*
55x75um	6M_4x1z	55um single
25x130um	7M_5x1z	25um dual
25x130um	9M_6x2z	25um dual
20x186um	9M_6x2z	20um triple

LIBRARY CELL SUMMARY

Cell Type	*Feature*
Supply / ESD	1.8/3.3V; 1.8V; 0.9V; GND
GPIO[1]	25, 75, 150 MHz, fail-safe
I2C Open-drain[2]	5V, fail-safe
HDMI[3]	3.3V, 5V tolerant, fail-safe
LVDS[3]	1.8V
Analog	1.8V & 3.3V
OTP	5V programming gate cell
Break cells	VDDIO, VDD, VSS
Filler cells	1um, 5um
Transition	Bridge to TSMC IOs

GPIO BLOCK DIAGRAM



GPIO FEATURES

- Multi-voltage 1.8V / 3.3V switchable operation
- 25MHz, 75MHz, & 150MHz GPIO[1] speed options
- Full-speed output enable
- Independent power sequencing
- Shorted output protection
- Schmitt trigger receiver
- 60KΩ selectable pull-up or pull-down resistor
- ESD: 2KV HBM, 500V CDM[4], 2KV IEC 61000-4-2[5]

Certus also supports IO libraries in the following TSMC nodes: 180nm, 130nm, 110nm, 65nm, 55nm, 45/40nm, 22nm, and 16/12nm. Additional Certus libraries are available across technologies supported by Global Foundries & Samsung. Certus is particularly suited at providing custom variants in a cost-efficient framework. Feel free to inquire for supplementary physical or electrical features to suit your needs.

1. GPIO speeds are load dependent (faster for lighter loads, slower for heavier). Speeds shown are at 10pF.
2. Open drain cell is I2C, SMBus, DDC, CEC, & HPD compliant.
3. Solution provides optimized low-capacitance ESD protection only.
4. CDM rating is a function of package size. Rating shown is for nominal packages.
5. Please contact a Certus representative for IEC 62100-4-2 protection levels achievable with your design.

