HDMI, LVDS, RF AND ANALOG PADS
IN TSMC 45/40nm TECHNOLOGY

A 1.0V to 5V Analog IO Library that includes an HDMI, LVDS, and Analog/RF Low Capacitance pad set in TSMC 45nm/40nm HPM processes.

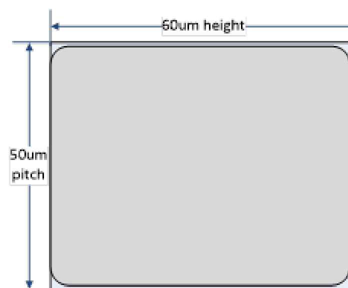
SUMMARY

This library is collection of analog only IO and Power/Ground pads that include ESD. The target applications are high performance analog interfaces including HDMI, RF, LVDS, basic analog and other applications. The pads include a host of specialty features including fail-safe, low capacitance, high ESD protection, and IEC robustness. The IO's are designed to trigger and protect interfaces during Electrical Overstress (EOS) events during normal operation. A key feature of the library is the extremely small footprint of the inline IO set, only 2.2um bigger than the bond pad itself. Capacitance can range from <150fF to 250fF and is scalable based on the customers' needs between ESD robustness and capacitive loading.

FEATURES

- In-line Low Cap Analog: 50um pitch x 60um height (HDMI, LVDS, RF, Analog, and Low-Cap IOs)
- Dual-row, staggered pitch of 25um x 150um height (Analog, RF, LVDS, and Low-Cap IOs)
- AVDD = 1.0V to 3.3V nominal, 5V tolerant HDMI option
- Capacitance 150fF to 250fF including bond pads*
- HBM >4000V*
- CDM >800V*
- MM >300V*
- IEC >2kV option*
- EOS protection
- Junction temperature range: -40˚C to 125˚C
- Can integrate with TSMC standard IO

BOND PAD & IO



The entire HDMI, RF and Analog In-Line cells are only 2.2um taller than the bond pads, completely CUP (Circuit Under Pad) and providing the industries smallest footprint for RF, Analog, and HDMI Low-Cap ESD and Pad Solutions.

HDMI AND LVDS PAD FEATURES

- Includes Power and GND pads
- <250fF per IO including Bondpad
- 1.8V to 3.3V power supply (HDMI)
- 1.8V Power Supply (LVDS and analog)
- 5V Tolerant (HDMI only)
- Fail-Safe IO (HDMI only
- Pad Macros provide for ideal parasitic matching between differential signal pins

MODELS AND SUPPORT FILES

- GDS layouts
- LEF Abstracts
- CDL netlist for simulation and LVS
- Functional models in behavioral Verilog with timing arcs

FRONT-END DEVICES

- 2.5V overdriven 3.3V thick-oxide NMOS and PMOS; No ESD implant layer or special masks required
- Back-end: Metal1 to Metal8, AP Bondpad layer for Wirebond, using Circuit-Under-Pad construction

Certus also supports IO libraries in the following TSMC nodes: 180nm, 130nm, 110nm, 65nm, 55nm, 28nm, 22nm, 16/12nm. Additional Certus libraries are available across technologies supported by GlobalFoundries & Samsung. Certus is particularly suited at providing custom variants in a cost-efficient framework. Feel free to inquire for supplementary physical or electrical features to suit your needs.

*: Capacitance and ESD robustness is a sliding scale, customers opting for lower capacitance do so at a cost of ESD robustness, and vice-versa. Nominal numbers listed are for 200-250fF Capacitive IO structures.

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