1.0V – 3.3V GPIO WITH I2C OPEN-DRAIN AND 3.3V & 5V ANALOG CELLS IN TSMC 55nm TECHNOLOGY

CERTUS semiconductor
CUSTOM IO AND ESD SOLUTIONS

A TSMC 55nm Wirebond IO library with 1-3.3V GPIO, 3.3V pulse-width modulation cell, I2C & SVID open-drain cells, 3.3V & 5V analog cells, OTP program cell & associated ESD

SUMMARY

Key attributes of this IO library include dual independent IO supply rails (1.0V-3.3V & 3.3V) and power-on-control (POC) to place IOs in HiZ during power-down. The GPIO cell can be configured as input, output or open-drain with a Schmitt trigger input and optional internal 55K ohm pull-up or pull-down resistor. Cells for two independent IO supplies, core power, ground and isolated ground with built-in ESD are included. A specialty output cell with matched throughput timings for pulse-width modulation (PWM) applications, along with 5V OTP programming, I2C & SVID open-drain and 3.3V & 5V analog cells (and associated ESD) complement the GPIO offering. The library is enriched with filler, corner and domain-break cells in digital and analog domains to allow for flexible pad ring construction. ESD design levels are 2KV HBM and 500V CDM.

OPERATING CONDITIONS

Parameter	*Value*
VDDIO	1-3.3V | 3.3V (dual rail)
Core VDD	1.2V
Tj	-40°C to 125°C
Max_Load	15pF

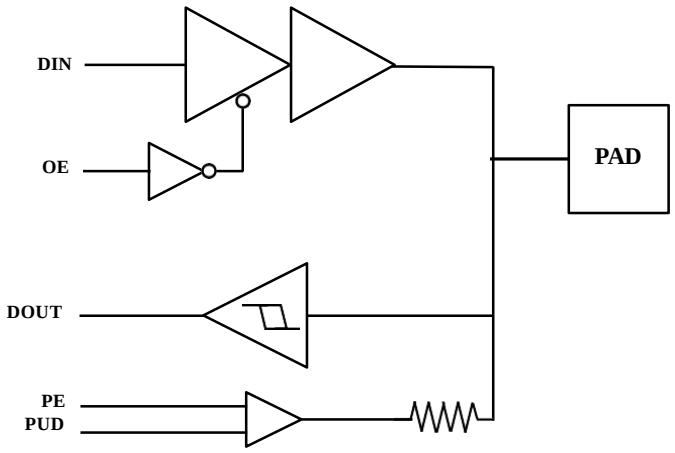
CELL SIZE & METAL STACK OPTIONS

Cell size	*Type*	*Metal Stack*	*WB pitch*
55x100um	Digital	1P7M – 1P9M	55um inline
55x76um	Analog		

LIBRARY CELL SUMMARY

Cell Type	*Feature*
Supply / ESD	1-3.3V & 3.3V IO; 1.2V core; GND
GPIO[1]	50MHz | 100MHz
PWM Output	Output cell w/ midrail disable
Power-On Ctrl	Sleep mode enable
I2C Open Drain	I2C and SVID variants
3.3V Analog	Substrate isolation option
5V Analog	Substrate isolation option
OTP	5V programming gate cell
Break cells	VDDIO, VDD, VSS
Filler cells	1um, 5um digital & analog
Corner	Digital & analog

GPIO BLOCK DIAGRAM



GPIO FEATURES

- 1.0V-3.3V | 3.3V IO operation
- Dual independent IO rails
- Output enable / disable (HiZ when disabled)
- Power-down control (HiZ upon VDD disable)
- Schmitt trigger receiver
- 55KΩ selectable pull-up or pull-down resistor
- ESD: 2KV HBM, 500V CDM[2]
- Silicon proven

Certus also supports IO libraries in the following TSMC nodes: 180nm, 130nm 110nm, 65nm, 45/40nm, 28nm, 22nm, and 16/12nm. Additional Certus libraries are available across technologies supported by Global Foundries & Samsung. Certus is particularly suited at providing custom variants in a cost-efficient framework. Feel free to inquire for supplementary physical or electrical features to suit your needs.

1. GPIO can sustain up to 50MHz on the 1-3.3V rail, 100MHz on the 3.3V rail (up to 10pF load)
2. CDM rating is a function of package size. Rating shown is for nominal packages.